

High Performance Sub-System Design and Assembly

B'D

Background of the Invention

Field of the Invention

This invention relates to structures and methods of assembly of integrated circuit chips into interconnected multiple chip circuits. More particularly, this invention relates to "chip-on-chip" structures connected physically and electrically.

Description of the Related Art

The manufacture of embedded Dynamic Random Access Memory (DRAM) requires that process parameters that enhance the performance of the logic or the DRAM, if separately formed on semiconductor chips, be compromised when DRAM is embedded into an array of logic gates on the same semiconductor chip. This compromise has limited the application of embedded DRAM. If there is no compromise in the process parameters to enhance the performance of logic or the DRAM embedded DRAM, the manufacture process becomes very complicated and costly. Moreover, because of the structure of the embedded DRAM and the logic, burn-in of the embedded DRAM is not possible and embedding of DRAM with logic is not a reliable design solution.

A "chip-on-chip" structure is a viable alternative to embedded DRAM. With multiple chips connected in intimate contact, the process parameters that maximize the performance of the DRAM chip and the logic gates can be applied during manufacture. Refer to Fig. 1 for a 5 description of a "chip-on-chip" structure **100**. Such a "chip-on-chip" structure is described in U.S. Patent 5,534,465 (Frye et al.). A first integrated circuit chip **105** is attached physically and electrically to a second integrated circuit chip **110** by means of an area array of solder bumps **115**. The process of forming an area array of solder bumps **115** is well known in the art and is discussed in Frye et al. 465. The second chip 10 110 is then secured physically to a substrate **120**. Electrical connections **125** between the second integrated circuit chip **110** and external circuitry (not shown) are created as either wire bonds or tape automated bonds. The module further has a ball grid array **130** to secure the structure to a 15 next level of packaging containing the external circuitry. Generally, an encasing material **135** is placed over the "chip-on-chip" structure **100** to provide environmental protection for the "chip-on-chip" **100**.

U.S. Patent 5,481,205 (Frye et al.) teaches a structure for making 20 temporary connections to integrated circuit chips having "solder bumps" or connection structures such as ball grid arrays. The temporary connections allow temporary contacting of the integrated circuit chip during testing of the integrated circuit chip.

The handling of wafers from which the integrated circuit chips are formed and the handling of the integrated circuit chip themselves causes the integrated circuit chips to be subjected to electrostatic discharge (ESD) voltages. Even though connections between the first integrated circuit chip **105** and the second integrated circuit chip **110** are relatively short and under normal operation would not be subjected to ESD voltages, require ESD protection circuitry to be formed within the interchip interface circuit to provide protection or necessary driving capacity for the first integrated circuit chip **105** and the second integrated circuit chip **110** during burn-in and other manufacturing monitoring processes.

U.S. Patent 5,731,945 and U.S. Patent 5,807,791 (Bertin et al.) teach a method for fabricating programmable ESD protection circuits for multichip semiconductor structures. The interchip interface circuit on each integrated circuit chip is formed with an ESD protection circuit and a switch to selectively connect the ESD protection circuit to an input/output pad. This allows multiple identical chips to be interconnected and redundant ESD protection removed.

20

The circuits at the periphery of integrated circuit chips generally are specialized to meet the requirements standardized specifications. These include relatively high current and voltage drivers and receivers for

communicating on relatively long transmission line media. Alternately, as shown in U.S. Patent 5,461,333 (Condon et al.) the interface may be differential to allow lower voltages on the transmission line media. This requires two input/output pads for transfer of signals.

5

U.S. Patent 5,818,748 (Bertin et al.) illustrates a separation of chip function onto separate integrated circuits chips. This allows the optimization of the circuits. In this case, EEPROM is on one integrated circuits chip and drivers and decoders are on another. The chips are placed face to face and secured with force responsive self-interlocking micro-connectors.

10
15

20

Figs. 2a and 2b show multiple "chip-on-chip" structures 100 constructed on a wafer. Not shown is the forming of the first integrated circuit chip on a silicon wafer. The first integrated circuit chip is tested on the wafer and nonfunctioning chips are identified. The wafer is separated into the individual chips. The functioning first integrated circuit chips 105 then are "flip-chip" mounted on the second integrated circuit chip 110 on the wafer 200. The wafer 200 is then separated into the "chip-on-chip" structures 100. The "chip-on-chip" structures 100 are then mounted on the modules as above described.

Summary of the Invention

An object of this invention is to provide a multiple integrated circuit chip structure where the interchip communication between integrated circuit chips of the structure have no ESD protection circuits and no input/output circuitry. The 5 interchip communication is between internal circuits with a minimal electrical load.

Another object of this invention is to provide a circuit to selectively connect internal circuits of the integrated circuits to test interface circuits having ESD 10 protection circuits and input/output circuitry designed to communicate with test systems during assembly and test.

To accomplish these and other objects, a multiple interconnected integrated circuit chip structure has a first integrated circuit chip mounted a 15 second integrated circuit chip to physically and electrically connect the first integrated circuit chip to the second integrated circuit chip. The first integrated circuit chip may be mounted to the second integrated circuit chip by means of an area array of solder bumps. The first integrated circuit chip has interchip interface circuits connected to the second integrated circuit chip to communicate 20 between internal circuits of the first and second integrated circuit chips and test circuits. The test circuits are connected to the internal circuits of the first integrated circuit chip to provide stimulus and response to the internal circuits during testing procedures.

The second integrated circuit chip has input/output interface circuitry to communicate with external circuitry connected to the second integrated circuit chip and to protect the second integrated circuit chip from electrostatic discharge
5 voltages. Further, the second integrated circuit has interchip interface circuits connected to the first integrated circuit chip to communicate between the internal circuits of the first and second integrated circuit chips, and with test circuits. The test circuits are connected to the internal circuits of the second integrated circuit chip to provide stimulus to and response from the internal circuits during testing
10 and burn-in procedures.

The interchip interface circuitry has an internal interface circuit for transferring electrical signals between the internal circuits of the second integrated circuit chip to the first integrated circuit chip. The interchip interface circuitry further has a mode select switch to selectively connect between the internal circuits of the first integrated circuits chip and the second integrated
15 circuits chip or to the test interface circuits. The mode switch has three terminals and a control terminal. The first terminal is connected to an output of the internal interface circuit, a second terminal connected to the internal circuitry, and the third terminal connected to test circuits. A mode selector is connected to the
20 control terminal. The state of the mode selector determines the connection between the first terminal and thus the output of the internal interface circuit, the second terminal and thus the internal circuitry, and the third terminal and thus the

test interface. During normal operation, the first terminal is connected to the second terminal such that the internal circuits of the first and second integrated circuits are connected through their respective internal interfaces. During test and burn-in, the internal circuits are connected to the test circuits.

5

The test circuits are formed of a test interface circuit and an ESD protection device. The test interface circuit connected to communicate test signals from external test circuitry to the first and second integrated circuit chips. The ESD protection device protects the first and second integrated circuit chips from electrostatic discharge voltages. The test interface circuit is connected to the external test circuitry through an input/output pad temporarily connected to the external test circuitry during test and burn-in.

The first integrated circuit chip could be fabricated using a first type of semiconductor process and the second integrated circuit chip would be fabricated with a second type of semiconductor process that is not compatible with the first type of semiconductor process. As an example, the first integrated circuit chip could be an array of memory cells and the second integrated circuit chip would contain electronic circuitry formed with a process not compatible with a process of the array of memory cells. Alternatively, the second integrated circuit chip is an array of memory cells and the first integrated circuit chip contains electronic circuitry formed with a process not compatible with a process of the array of memory cells. Fabricating the first integrated circuit chip using its

optimum semiconductor process, fabricating the second integrated circuit chip using its optimum semiconductor process, and then joining the first and second integrated circuit chips by this invention creates a multiple chip integrated circuit structure having maximum performance with minimum cost.

5

Brief Description of the Drawings

Fig. 1 shows a cross-sectional view of a "chip-on-chip" structure of the prior art.

10 Figs. 2a and 2b are respectively top view and a cross-sectional view of a "chip-on-chip" structure formed on a semiconductor wafer of the prior art.

15 Fig. 3 is a cross-sectional view of a "chip-on-chip" structure, schematically the circuitry contained on each chip of the chip-on-chip structure of this invention.

20 Figs. 4 a-d are schematics of the interchip interface circuits of this invention.

Figs. 5a and 5b are schematic drawings of an embodiment of the interchip interface of this invention.

Figs. 6a and 6b are top surface views of the first and second integrated circuit chips of Fig. 3 showing test pads and interchip input/output pads of this invention.

5

Detailed Description of the Invention

A "chip-on-chip" structure **300** is shown in Fig. 3. A first integrated circuit chip **305** is attached to a second integrated circuit chip **310** by means of an area array of solder bumps **315** as described above. The second integrated circuit chip **310** is secured physically to the module **320**. The electrical connections **325** are either wire bonds or TAB bonds. The module **320** has a ball grid array **330** to attach the "chip-on-chip" structure within the module to a next level of electronic package.

10

15

15

15

20

The first integrated circuit chip **305** has internal circuits **335**, which are the functional electronic components of the first integrated circuit chip **305**. The internal circuits **335** may be DRAM, logic, or other integrated circuits. Likewise, the second integrated circuit chip **310** has the internal circuits **365**. The internal circuits **365** are the functional electronic components of the second integrated circuit chips **310**. These internal circuits also may be DRAM, logic, or other integrated circuits. To transfer signals between the internal circuits **335** of the first integrated circuit chip **305** and the internal circuits **365** of the second chip **310** or to an external test system, the internal circuits **335** are connected to the interchip interface circuits **340**. The interchip interface circuits **340** are connected

through the input/output pads **345** to the area array of solder bumps **315** and thus to the second chip **310**. This connection is functional during normal operation, when the first integrated circuit chip **305** is mounted to the second integrated circuit chip **310**.

5

The interchip interface circuit **340** also is connected to the test interface **350**. The test interface circuit **350** is connected to the test input/output pads **355**. The test interface circuit **350** is functionally active during testing procedures, when test system probes are brought in contact with the test input/output pads **355**. The test system probes provide test stimuli and receive response from the internal circuits **335**.

The mode select **390** for the first integrated circuit chip **305** is accomplished by placing an appropriate logic level on the mode select input/output pads **391** and **392**. When the first integrated circuit chip **305** is in contact with a test system during wafer testing or die testing during burn-in, the mode select input/output pad **391** is brought to a first logic level (0) to cause the interchip interface circuit **340** to transfer signals between the internal circuits **335** and the test interface **350**. The test signals are then transferred between the test interface **350** and the test input/output pad **355** as described above.

When the first integrated circuit chip **305** is mounted to the second integrated circuit chip **310**, the mode select line **390** is brought to a second logic

level (1) through the mode select input/output pad **392**. The second logic level (1) is a voltage equal to the power supply voltage source **V_{DD}** and is achieved by connecting the mode select input output pad **392** to the mode select input/output pad **393** on the second integrated circuit chip **310** through the solder ball **394**.

5 The mode select input/output pad **393** is connected directly to the power supply voltage source **V_{DD}** to achieve the second logic level (1). When the mode select line **390** is at the second logic level (1), the interchip interface **340** transfers signals of the internal circuits **335** to the input/output pads **345** to the second integrated circuit chip **310** as described above.

10

The internal circuits **365** of the second integrated circuit chip **310** likewise are connected to the interchip interface circuits **360**. The interchip interface circuits **360** are connected to the input/output pads **370** and thus to the first integrated circuit chip **310** through the area array of solder bumps **315**. The 15 interchip interface circuits **360** are connected to the test interface circuits **375**.

10 The internal circuits **365** of the second integrated circuit chip **310** are connected to the input/output interface **385**. The input/output interface is connected to the input/output pad **395**, which is connected to the module **320** 20 through the bondwire **325**. The input/output interface provides the circuitry to transfer signals between the internal circuits **365** and the external circuits attached through the next packaging level to the ball grid array **330** and thus to the wirebond **325**.

The second integrated circuit chip 310 is tested prior to separation of a wafer containing the second integrated circuit chip 310, by bringing test probes or needles of the test system in contact with the input/output pads 395 and the test 5 input/output pads 377. Subsequent to dicing of the wafer into individual second integrated circuit chips 310, the individual second integrated circuit chips 310 are mounted in a burn-in apparatus. The burn-in apparatus again is brought in contact with the input/output pads 395 and the test input/output pads 377 to provide stressing signals to the circuits of the second integrated circuit chip 310.

10 Then, when the first integrated circuit chip 305 is mounted to the second integrated circuit chip 310, operation of the whole "chip-on-chip" assembly 300 is verified by attaching testing probes or contacts to the ball grid array 330. Signals from the testing probes are transferred between the circuits of the whole "chip-on-chip" assembly 300 through the bond wires 325 to the input/output pads 395.

15 The mode select 380 for the second integrated circuit chip 310 is accomplished by placing an appropriate logic level on the mode select input/output pads 381 and 382. When the second integrated circuit chip 310 is in contact with a test system during wafer testing or die testing during burn-in, the 20 mode select input/output pad 381 is brought to a first logic level (0) to cause the interchip interface circuit 360 to transfer signals between the internal circuits 365 and the test interface 375. The test signals are then transferred between the test interface 375 and the test input/output pad 377 as described above.

When the first integrated circuit chip **305** is mounted to the second integrated circuit chip **310**, the mode select line **380** is brought to a second logic level (1) through the mode select input/output pad **382**. The second logic level (1) is achieved by connecting the mode select input output pad **382** to the mode select input/output pad **383** on the ^{first} _{second} integrated circuit chip **310** through the solder ball **384**. The mode select input/output pad **383** is connected directly to the power supply voltage source **V_{DD}** to achieve the second logic level (1). When the mode select line **380** is at the second logic level (1), the interchip interface **360** transfers signals of the internal circuits **365** to the input/output pads **370** to the first integrated circuit chip **305** as described above.

The input/output interface circuit **385** has an input/output buffer **389** connected to the internal circuits **365**. The input/output buffer **389** is either a driver or receiver necessary to translate the signal levels of the internal circuits **365** to the signal levels of the external circuits and the signal levels of the external circuits to the signal levels of the internal circuit **365**. The input/output buffer is connected to the input/output pad **395** and to the ESD protection circuit **387**. The ESD protection circuit **387** clamps excess ESD voltages to prevent damage to the input/output buffer **389** and the internal circuits **365** from ESD voltages brought in contact with the input/output pad **395** from the external environment.

Figs. 4a and 4d show schematically the connections of the interchip interface **340** and the test interface **350** of the first integrated circuit chip **305** of Fig. 3. Fig. 4a illustrates a path of a signal originated within the internal circuits **400** of the first integrated circuit chip and Fig. 4d illustrates a path of a signal originated externally and received by the internal circuits **462** of the first integrated circuit chip.

Referring now to Fig. 4a, the interchip interface **340** is comprised of a mode switch **402** and a mode selector **404**. The signal **400** originating from the internal circuit of the first integrated circuit chip is connected to a first terminal of the mode switch **402**. The second terminal of the mode switch **402** is connected directly to an input/output pad of the first integrated circuit chip and thus to the internal circuits of the second integrated circuit chip, as described above. The third terminal of the mode switch **402** is connected to the test interface **350**. The test interface circuit **350** is composed of the test circuit **406** connected to an input of a driver circuit **410**.

The output of the driver circuit is connected to a test input/output pad **412** and to the ESD protection circuit **414**. The ESD protection circuit **414** operates as the ESD protection circuit **387** of Fig. 3 and clamps excessive ESD voltage to protect the test interface circuit **350** from damage during handling of the wafer containing the first integrated circuit chip for manufacturing, assembly, and testing.

The control terminal of the mode switch **402** is connected to a mode selector **404** to control the function of the interchip interface **340**. When the mode selector **404** is at a first logic state, the internal circuits **400** of the first integrated circuit chip are connected to the input/output **408** and thus to the internal circuits of the second integrated circuit chip. When the mode selector **404** is at a second logic state, the internal circuits **400** of the first integrated circuit chip are connected to the test interface circuit **350**. The mode selector **404** is set to the second state during the testing procedures of the wafer containing the first integrated circuit chip. Conversely, when the mode selector **404** is set to the first logic state during the normal operation of the "chip-on-chip" structure.

Referring to Fig. 4d, the signals originating in the internal circuits of the second integrated circuit chip are transferred to the chip pad **454** of the first integrated circuit. The chip pad **454** is connected to the first terminal of the mode switch **456**. The test interface circuit **350** is connected to the second terminal of the mode switch **456**. The third terminal of the mode switch **456** is connected to the internal circuits **462** of the first integrated circuit chip. The control terminal of the mode switch **456** is connected to the mode selector **458** to control the function of the interchip interface **340**. If the control terminal of the mode switch **458** is at the first logic state, the chip pad **454** of the first integrated circuit chip and thus internal circuits of the second integrated circuit chip are connected to

the internal circuits of the first integrated circuit chip. Conversely, if the control terminal of the mode switch **458** is at the second logic state, the test interface circuit **350** is connected to the internal circuit of the first integrated circuit chip.

5 As described above, the mode selector **458** is set to the second logic state during the testing procedures of the wafer containing the first integrated circuit chip and the mode selector **458** is set to the first logic state during the normal operation of the "chip-on-chip" structure.

10 Figs. 4b and 4c show schematically the connections of the interchip interface **360** and the test interface **375** of the second integrated circuit chip **310** of Fig. 3. Fig. 4b illustrates a path of a signal originated within the internal circuits **430** of the second integrated circuit chip and Fig. 4c illustrates a path of a signal originated externally and received by the internal circuits **432** of the second integrated circuit chip.

15 Fig. 4b shows the instance where the signals originate on the first integrated circuit chip and are transferred through to the input/output pad **422** of the second integrated circuit chip. The input/output pad **422** is connected to the first terminal of the mode switch **424**. The test interface circuit **375** is connected to the second terminal of the mode switch **424**. The third terminal of the mode switch **424** is connected to the internal circuits **430** of the second integrated circuit chip. The control terminal of the mode switch **424** is connected to the

mode selector **426**, which operates as described above. If the mode selector **426** is at the first logic state, the signals from the internal circuit of the first integrated circuit chip are connected through the input/output pad **422** to the internal circuits **430** of the second integrated circuit chip. Alternately, if the mode selector is at the second logic state, the test signals from an external test system are transferred through the test interface **350** to the internal circuits **430** of the second integrated circuit chip. Again, as described above, the mode selector **426** is set to the first logic state during normal operation and is set to the second logic state during testing procedures.

The test interface is similar to that described in Fig. 4d. The test signals originating in an external test system are applied to a test input/output pad **416**. The test input/output pad **416** is connected to a receiver **420** an ESD protection circuit **418**. The receiver **420** translates the test signals to signal levels acceptable by the test circuit **428** and the internal circuits **430** of the second integrated circuit chip.

The ESD protection circuit **418** clamps ESD voltages applied to the test pad **416** to prevent damage to the second integrated circuit chip. The test circuits **428** format the test signals for application to the internal circuits **436** of the second integrated circuit chip.

Fig. 4c shows the instance where the signals originate in the internal circuits **432** of the second integrated circuit chip and are transferred through chip pad **438** to the first integrated circuit chip. The first terminal of the mode switch **436** receives the signals from the internal circuits **432** of the second integrated circuit chip. The second terminal of the mode switch **436** is connected to the chip pad **438**. The third terminal is connected to the test interface **375**. The control terminal is connected to the mode selector **434**.

As described above, the mode selector **434** determines the connection of the internal circuits **432** to either the chip pad **438** or the test interface circuit **375**. If the mode selector **434** is at the first logic state, the internal circuits **432** are connected through the chip pad **438** to the internal circuits of the first integrated circuit chip. Alternately, if the mode selector **434** is set to the second logic state, the internal circuits **432** are connected to the test interface circuit **375**.

The mode selector **434** is set to the first logic state during normal system operation and to the second logic state during testing procedures.

Figs. 5a and 5b illustrate the structure of an embodiment of the mode switch and the mode selector shown in Figs. 3 and 4 a-d. Fig. 5a shows the mode switch **500** and mode selector **520** for signals originated from the internal circuits **508** from the first or second integrated circuit chips. Alternately, Fig. 5b shows the mode switch **500** and mode selector **520** for signals originated

externally and transferred to the internal circuits **508** of the first or second integrated circuit chips.

Referring now to Fig. 5a, the first terminal of the mode switch **500** is
5 connected to the internal circuits **508**, the second terminal of the mode switch **500** is connected to the test interface circuit **510** and the third terminal of the mode switch **500** is connected to the interchip input/output pad **530**.

The mode switch is comprised of the pass switches **502** and **504** and inverter **506**. The pass switch **502** is the parallel combination of the n-channel metal oxide semiconductor (NMOS) transistor **502a** and p-channel metal oxide semiconductor (PMOS) transistor **502b**. Likewise, the pass switch **504** is the parallel combination of the NMOS transistor **504a** and the PMOS transistor **504b**.
10 The first terminal of the mode switch **500** and thus the internal circuits **508** are connected to the drains of the pass switches **502** and **504**. The sources of the pass switch **502** are connected to the third terminal of the mode switch **500** and thus to the interchip input/output pad **530**. The sources of the pass switch **504** are connected to the second terminal of the mode switch **500** and thus to the test interface circuit **510**. The gates of the NMOS transistor **504a** and the PMOS
15 transistor **502b** are connected to the output of the inverter **506**. The gates of the NMOS transistor **502a**, PMOS transistor **504b**, and the input of the inverter **506** are connected to the control terminal of the mode switch **500** and thus to the mode selector **520**.
20

When the control terminal of the mode switch **500** is at the first logic state, in this case a voltage level approaching that of the power supply voltage source V_{DD} , the pass switch **502** is turned on and the pass switch **504** is turned off. This 5 effectively connects the internal circuits **508** to the interchip input/output pad **530**. In this logic state, the extra electrical load is from the drain of the pass switch **502** and the pass switch **504**. This electrical load is very small and thus highly improved performance can be expected over the prior art. Conversely, when the control terminal of the mode switch **500** is at the second logic state, in this case a 10 voltage level approaching that of the substrate biasing voltage source V_{ss} , the pass switch **504** is turned on and the pass switch **502** is turned off. The internal circuits are now effectively connected to the test interface circuit **510**.

15 The test interface circuit **510** is comprised of the test circuit **512**, the driver circuit **514**, and the ESD protection circuit **516**. The test interface circuit functions as described in Figs. 4a and 4c.

20 The mode select circuit is the interchip input/output pad **522** and the test input/output pad **524** connected together and to the control terminal of the mode switch **500**. The interchip input/output pad **522** is connected as described in Fig. 3 to a mating interchip input/output pad **562** that are joined by a solder bump or ball. The mating interchip input/output pad **562** is on the mating chip **560** and is connected to the power supply voltage source V_{DD} to provide the first logic state

to the control terminal of the mode switch **500** during normal operation. The test input/output pad is connected to the test system **550** during the testing procedures. During the test procedures, a test probe or needle **552** is brought in contact with the test input/output pad. The test probe or needle **552** is connected 5 on a probe card **554** within the test system **550** to the substrate biasing voltage source V_{ss} to provide the second logic state to the control terminal of the mode switch **500**.

10 The fundamental connections shown in Fig. 5b are as described in Fig. 5a except the test signal originates from the test system attached to the input/output pad **540**. The test interface circuit **510** in this case is comprised of the test circuits **512**, the receiver **518**, and the ESD protection circuit and functions as 15 described in Figs. 4b and 4d.

15 Signals originating from the external circuits are applied to the interchip input/output pad **530** and transferred through the pass switch **502** to the internal circuits **508** during normal operation. Likewise, the test signals are transferred from the test interface **510** through the pass switch **504** to the internal circuits **508** during the test procedures.

20

Fig. 6a shows a top surface view of the first integrated circuit chip **600** illustrating the placement of the test input/output pads **605** and the interchip input/output pads **610**. The interchip input/output pads **610** form an area array of

solder balls or bumps **315** of Fig. 3. The test input/output pads **605** are peripherally arranged so that the test probes or needles of the test system can conveniently make contact with the test input/output pads **605**.

5 Fig. 6b shows the top surface view of the second integrated circuit chip **615** illustrating the placement of the interchip input/output pads **625** and the external input/output pads **620**. The interchip input/output pads **625** form the area array to mate with the interchip input/output pads **610** of Fig. 5a. The first integrated circuit chip **600** is mounted "face-to face" to the second integrated circuit chip **615**. The test input/output pads **605** must have nothing on the surface of the second integrated circuit chip **625** in their "shadow."

10
15
20
25
30
35
40
45
50
55
60
65
70
75
80
85
90
95
100
105
110
115
120
125
130
135
140
145
150
155
160
165
170
175
180
185
190
195
200
205
210
215
220
225
230
235
240
245
250
255
260
265
270
275
280
285
290
295
300
305
310
315
320
325
330
335
340
345
350
355
360
365
370
375
380
385
390
395
400
405
410
415
420
425
430
435
440
445
450
455
460
465
470
475
480
485
490
495
500
505
510
515
520
525
530
535
540
545
550
555
560
565
570
575
580
585
590
595
600
605
610
615
620
625
630
635
640
645
650
655
660
665
670
675
680
685
690
695
700
705
710
715
720
725
730
735
740
745
750
755
760
765
770
775
780
785
790
795
800
805
810
815
820
825
830
835
840
845
850
855
860
865
870
875
880
885
890
895
900
905
910
915
920
925
930
935
940
945
950
955
960
965
970
975
980
985
990
995
1000
1005
1010
1015
1020
1025
1030
1035
1040
1045
1050
1055
1060
1065
1070
1075
1080
1085
1090
1095
1100
1105
1110
1115
1120
1125
1130
1135
1140
1145
1150
1155
1160
1165
1170
1175
1180
1185
1190
1195
1200
1205
1210
1215
1220
1225
1230
1235
1240
1245
1250
1255
1260
1265
1270
1275
1280
1285
1290
1295
1300
1305
1310
1315
1320
1325
1330
1335
1340
1345
1350
1355
1360
1365
1370
1375
1380
1385
1390
1395
1400
1405
1410
1415
1420
1425
1430
1435
1440
1445
1450
1455
1460
1465
1470
1475
1480
1485
1490
1495
1500
1505
1510
1515
1520
1525
1530
1535
1540
1545
1550
1555
1560
1565
1570
1575
1580
1585
1590
1595
1600
1605
1610
1615
1620
1625
1630
1635
1640
1645
1650
1655
1660
1665
1670
1675
1680
1685
1690
1695
1700
1705
1710
1715
1720
1725
1730
1735
1740
1745
1750
1755
1760
1765
1770
1775
1780
1785
1790
1795
1800
1805
1810
1815
1820
1825
1830
1835
1840
1845
1850
1855
1860
1865
1870
1875
1880
1885
1890
1895
1900
1905
1910
1915
1920
1925
1930
1935
1940
1945
1950
1955
1960
1965
1970
1975
1980
1985
1990
1995
2000
2005
2010
2015
2020
2025
2030
2035
2040
2045
2050
2055
2060
2065
2070
2075
2080
2085
2090
2095
2100
2105
2110
2115
2120
2125
2130
2135
2140
2145
2150
2155
2160
2165
2170
2175
2180
2185
2190
2195
2200
2205
2210
2215
2220
2225
2230
2235
2240
2245
2250
2255
2260
2265
2270
2275
2280
2285
2290
2295
2300
2305
2310
2315
2320
2325
2330
2335
2340
2345
2350
2355
2360
2365
2370
2375
2380
2385
2390
2395
2400
2405
2410
2415
2420
2425
2430
2435
2440
2445
2450
2455
2460
2465
2470
2475
2480
2485
2490
2495
2500
2505
2510
2515
2520
2525
2530
2535
2540
2545
2550
2555
2560
2565
2570
2575
2580
2585
2590
2595
2600
2605
2610
2615
2620
2625
2630
2635
2640
2645
2650
2655
2660
2665
2670
2675
2680
2685
2690
2695
2700
2705
2710
2715
2720
2725
2730
2735
2740
2745
2750
2755
2760
2765
2770
2775
2780
2785
2790
2795
2800
2805
2810
2815
2820
2825
2830
2835
2840
2845
2850
2855
2860
2865
2870
2875
2880
2885
2890
2895
2900
2905
2910
2915
2920
2925
2930
2935
2940
2945
2950
2955
2960
2965
2970
2975
2980
2985
2990
2995
3000
3005
3010
3015
3020
3025
3030
3035
3040
3045
3050
3055
3060
3065
3070
3075
3080
3085
3090
3095
3100
3105
3110
3115
3120
3125
3130
3135
3140
3145
3150
3155
3160
3165
3170
3175
3180
3185
3190
3195
3200
3205
3210
3215
3220
3225
3230
3235
3240
3245
3250
3255
3260
3265
3270
3275
3280
3285
3290
3295
3300
3305
3310
3315
3320
3325
3330
3335
3340
3345
3350
3355
3360
3365
3370
3375
3380
3385
3390
3395
3400
3405
3410
3415
3420
3425
3430
3435
3440
3445
3450
3455
3460
3465
3470
3475
3480
3485
3490
3495
3500
3505
3510
3515
3520
3525
3530
3535
3540
3545
3550
3555
3560
3565
3570
3575
3580
3585
3590
3595
3600
3605
3610
3615
3620
3625
3630
3635
3640
3645
3650
3655
3660
3665
3670
3675
3680
3685
3690
3695
3700
3705
3710
3715
3720
3725
3730
3735
3740
3745
3750
3755
3760
3765
3770
3775
3780
3785
3790
3795
3800
3805
3810
3815
3820
3825
3830
3835
3840
3845
3850
3855
3860
3865
3870
3875
3880
3885
3890
3895
3900
3905
3910
3915
3920
3925
3930
3935
3940
3945
3950
3955
3960
3965
3970
3975
3980
3985
3990
3995
4000
4005
4010
4015
4020
4025
4030
4035
4040
4045
4050
4055
4060
4065
4070
4075
4080
4085
4090
4095
4100
4105
4110
4115
4120
4125
4130
4135
4140
4145
4150
4155
4160
4165
4170
4175
4180
4185
4190
4195
4200
4205
4210
4215
4220
4225
4230
4235
4240
4245
4250
4255
4260
4265
4270
4275
4280
4285
4290
4295
4300
4305
4310
4315
4320
4325
4330
4335
4340
4345
4350
4355
4360
4365
4370
4375
4380
4385
4390
4395
4400
4405
4410
4415
4420
4425
4430
4435
4440
4445
4450
4455
4460
4465
4470
4475
4480
4485
4490
4495
4500
4505
4510
4515
4520
4525
4530
4535
4540
4545
4550
4555
4560
4565
4570
4575
4580
4585
4590
4595
4600
4605
4610
4615
4620
4625
4630
4635
4640
4645
4650
4655
4660
4665
4670
4675
4680
4685
4690
4695
4700
4705
4710
4715
4720
4725
4730
4735
4740
4745
4750
4755
4760
4765
4770
4775
4780
4785
4790
4795
4800
4805
4810
4815
4820
4825
4830
4835
4840
4845
4850
4855
4860
4865
4870
4875
4880
4885
4890
4895
4900
4905
4910
4915
4920
4925
4930
4935
4940
4945
4950
4955
4960
4965
4970
4975
4980
4985
4990
4995
5000
5005
5010
5015
5020
5025
5030
5035
5040
5045
5050
5055
5060
5065
5070
5075
5080
5085
5090
5095
5100
5105
5110
5115
5120
5125
5130
5135
5140
5145
5150
5155
5160
5165
5170
5175
5180
5185
5190
5195
5200
5205
5210
5215
5220
5225
5230
5235
5240
5245
5250
5255
5260
5265
5270
5275
5280
5285
5290
5295
5300
5305
5310
5315
5320
5325
5330
5335
5340
5345
5350
5355
5360
5365
5370
5375
5380
5385
5390
5395
5400
5405
5410
5415
5420
5425
5430
5435
5440
5445
5450
5455
5460
5465
5470
5475
5480
5485
5490
5495
5500
5505
5510
5515
5520
5525
5530
5535
5540
5545
5550
5555
5560
5565
5570
5575
5580
5585
5590
5595
5600
5605
5610
5615
5620
5625
5630
5635
5640
5645
5650
5655
5660
5665
5670
5675
5680
5685
5690
5695
5700
5705
5710
5715
5720
5725
5730
5735
5740
5745
5750
5755
5760
5765
5770
5775
5780
5785
5790
5795
5800
5805
5810
5815
5820
5825
5830
5835
5840
5845
5850
5855
5860
5865
5870
5875
5880
5885
5890
5895
5900
5905
5910
5915
5920
5925
5930
5935
5940
5945
5950
5955
5960
5965
5970
5975
5980
5985
5990
5995
6000
6005
6010
6015
6020
6025
6030
6035
6040
6045
6050
6055
6060
6065
6070
6075
6080
6085
6090
6095
6100
6105
6110
6115
6120
6125
6130
6135
6140
6145
6150
6155
6160
6165
6170
6175
6180
6185
6190
6195
6200
6205
6210
6215
6220
6225
6230
6235
6240
6245
6250
6255
6260
6265
6270
6275
6280
6285
6290
6295
6300
6305
6310
6315
6320
6325
6330
6335
6340
6345
6350
6355
6360
6365
6370
6375
6380
6385
6390
6395
6400
6405
6410
6415
6420
6425
6430
6435
6440
6445
6450
6455
6460
6465
6470
6475
6480
6485
6490
6495
6500
6505
6510
6515
6520
6525
6530
6535
6540
6545
6550
6555
6560
6565
6570
6575
6580
6585
6590
6595
6600
6605
6610
6615
6620
6625
6630
6635
6640
6645
6650
6655
6660
6665
6670
6675
6680
6685
6690
6695
6700
6705
6710
6715
6720
6725
6730
6735
6740
6745
6750
6755
6760
6765
6770
6775
6780
6785
6790
6795
6800
6805
6810
6815
6820
6825
6830
6835
6840
6845
6850
6855
6860
6865
6870
6875
6880
6885
6890
6895
6900
6905
6910
6915
6920
6925
6930
6935
6940
6945
6950
6955
6960
6965
6970
6975
6980
6985
6990
6995
7000
7005
7010
7015
7020
7025
7030
7035
7040
7045
7050
7055
7060
7065
7070
7075
7080
7085
7090
7095
7100
7105
7110
7115
7120
7125
7130
7135
7140
7145
7150
7155
7160
7165
7170
7175
7180
7185
7190
7195
7200
7205
7210
7215
7220
7225
7230
7235
7240
7245
7250
7255
7260
7265
7270
7275
7280
7285
7290
7295
7300
7305
7310
7315
7320
7325
7330
7335
7340
7345
7350
7355
7360
7365
7370
7375
7380
7385
7390
7395
7400
7405
7410
7415
7420
7425
7430
7435
7440
7445
7450
7455
7460
7465
7470
7475
7480
7485
7490
7495
7500
7505
7510
7515
7520
7525
7530
7535
7540
7545
7550
7555
7560
7565
7570
7575
7580
7585
7590
7595
7600
7605
7610
7615
7620
7625
7630
7635
7640
7645
7650
7655
7660
7665
7670
7675
7680
7685
7690
7695
7700
7705
7710
7715
7720
7725
7730
7735
7740
7745
7750
7755
7760
7765
7770
7775
7780
7785
7790
7795
7800
7805
7810
7815
7820
7825
7830
7835
7840
7845
7850
7855
7860
7865
7870
7875
7880
7885
7890
7895
7900
7905
7910
7915
7920
7925
7930
7935
7940
7945
7950
7955
7960
7965
7970
7975
7980
7985
7990
7995
8000
8005
8010
8015
8020
8025
8030
8035
8040
8045
8050
8055
8060
8065
8070
8075
8080
8085
8090
8095
8100
8105
8110
8115
8120
8125
8130
8135
8140
8145
8150
8155
8160
8165
8170
8175
8180
8185
8190
8195
8200
8205
8210
8215
8220
8225
8230
8235
8240
8245
8250
8255
8260
8265
8270
8275
8280
8285
8290
8295
8300
8305
8310
8315
8320
8325
8330
8335
8340
8345
8350
8355
8360
8365
8370
8375
8380
8385
8390
8395
8400
8405
8410
8415
8420
8425
8430
8435
8440
8445
8450
8455
8460
8465
8470
8475
8480
8485
8490
8495
8500
8505
8510
8515
8520
8525
8530
8535
8540
8545
8550
8555
8560
8565
8570
8575
8580
8585
8590
8595
8600
8605
8610
8615
8620
8625
8630
8635
8640
8645
8650
8655
8660
8665
8670
8675
8680
8685
8690
8695
8700
8705
8710
8715
8720
8725
8730
8735
8740
8745
8750
8755
8760
8765
8770
8775
8780
8785
8790
8795
8800
8805
8810
8815
8820
8825
8830
8835
8840
8845
8850
8855
8860
8865
8870
8875
8880
8885
8890
8895
8900
8905
8910
8915
8920
8925
8930
8935
8940
8945
8950
8955
8960
8965
8970
8975
8980
8985
8990
8995
9000
9005
9010
9015
9020
9025
9030
9035
9040
9045
9050
9055
9060
9065
9070
9075
9080
9085
9090
9095
9100
9105
9110
9115
9120
9125
9130
9135
9140
9145
9150
9155
9160
9165
9170
9175
9180
9185
9190
9195
9200
9205
9210
9215
9220
9225
9230
9235
9240
9245
9250
9255
9260
9265
9270
9275
9280
9285
9290
9295
9300
9305
9310
9315
9320
9325
9330
9335
9340
9345
9350
9355
9360
9365

While this invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

5

The invention claimed is: